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TITLE: A 360° DIGITAL PHASE DETECTOR WITH 100-kHZ BANDWIDTH

MASTER

AUTHOR(S): D. W. Reid, D. Riggin, M. V. Fazio, R. S. Biddle,
R. C. Patton, and H. A. Jackson

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A 360° DIGITAL PHASE DETECTOR WITH 100-kHz BANDWIDTH*

D. W. Reid, D. Riggin, M. V. Fazio, R. S. Biddle, R. D. Patton, and H. A. Jackson
Los Alamos National Laboratory, Los Alamos, NM

Summary

The general availability of digital circuit components with propagation delay times of a few nanoseconds makes a digital phase detector with good bandwidth feasible. Such a circuit has a distinct advantage over its analog counterpart because of its linearity over a wide range of phase shift.

This paper describes a phase detector that is being built at Los Alamos National Laboratory for the Fusion Materials Irradiation Test (FMIT) project. The specifications are 100-kHz bandwidth, linearity of ± 1° over ± 180° of phase shift, and 0.66° resolution. To date, the circuit has achieved the bandwidth and resolution. The linearity is approximately ± 3° over ± 180° phase shift.

Design

The basic theory of the phase detector is that of a digital integrator. A pulse, V_z with width linearly proportional to the phase difference between a reference square wave (V_{ref}) and a signal square wave (V_{sig}) can be generated with appropriate signal processing. V_{ref} and V_{sig} are at the same frequency, f_o, but V_{sig} is shifted in phase by ± Θ. Further, if V_z is filled with a series of pulses whose frequency, f_1, is much greater than f_o, then in theory, counting the pulses enclosed by V_z is a direct measure of the phase shift. Furthermore, to the extent that f_o and f_1 are stable frequencies, the system is linear and can easily measure ± 180° phase shift.

The timing diagram for the pulse orientation is shown in Fig. 1 for the case in which V_{sig} lags V_{ref}, and for which V_{sig} leads V_{ref}. It is apparent from the diagram that the full ± 180° of phase information is contained in half of the 100-kHz square wave, leaving the other half for appropriate signal processing, sample-and-hold, D-to-A conversion, etc.

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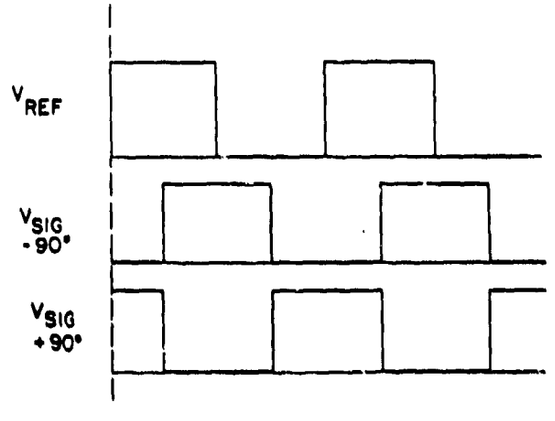

Fig. 1. V_{sig} versus V_{ref}.

The system's bandwidth is defined as the rate at which phase shift is detected. It also is useful to define a parameter, system resolution R, as follows:

$$R = \frac{360}{f_1/BW} \text{ degrees per pulse} .$$

Because this is a digital integration system, one pulse is the minimum unit that can be counted. Thus, maximum sensitivity occurs with a relatively small bandwidth and a high pulse-train frequency f_1, which yields the minimum degrees per pulse. There is one practical consideration, however; f_1 must be counted by fast binary counters. This puts a practical upper limit on f_1 of about 100 MHz. In the circuit being discussed, f_1 was chosen to be 50 MHz and the bandwidth was chosen to be 100 kHz. Thus, the system resolution is 0.66° per pulse.

Figure 2 is a block diagram of a digital phase detector that satisfies the criteria discussed above.

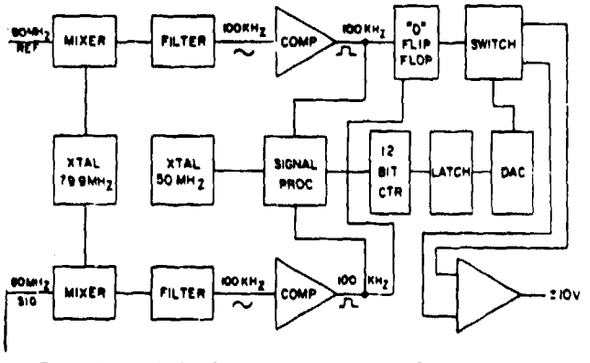

Fig. 2. Digital phase detector block diagram.

The incoming V_{ref} and V_{sig}, in this case at 80 MHz, are mixed with a crystal source at 79.9 MHz and the difference frequency is fed into the comparators that are used as zero-crossing detectors. The comparators' output is 100-kHz square waves. These are fed, along with the 50-MHz pulse train, into a signal-processing stage that generates a burst of 50-MHz pulses. The width of the burst is directly proportional to the phase difference between V_{ref} and V_{sig}. The burst of 50-MHz pulses is generated with the circuitry shown in Fig. 3. The timing diagram for the resultant signals is shown in Fig. 4.

The output from the signal processing stage is fed to a 12-bit binary counter that counts the number of pulses in a burst. The number of pulses is linearly proportional to the phase shift. During the interpulse time, and using appropriate pulse timing circuitry, this count is transferred to a fast D-to-A converter, where the analog output is held until the next pulse cycle.

An examination of Fig. 4 shows that the digital integrater cannot discern between a leading and lagging pulse. The "D" flip-flop and solid-state switch provides the lead or lag discernment capability. The V_{ref} is connected to the clock input, and V_{sig} is connected to the D input. If the V_{sig} is leading, the Q output is high. If lagging, the Q output is low. By feeding this signal to the solid state switch, the output of the DAC is toggled to the inverting or noninverting

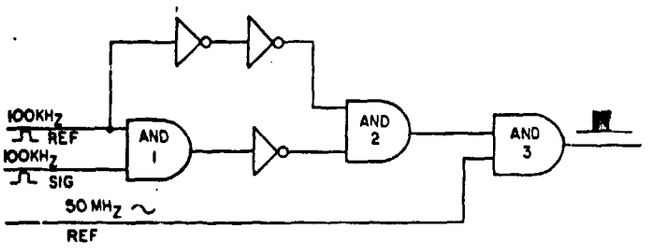

Fig. 3. Signal processor block diagram.

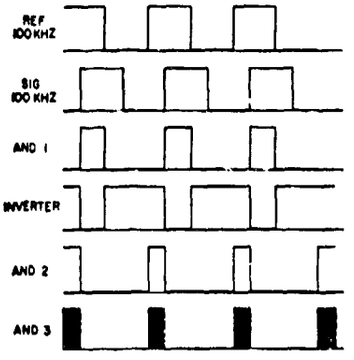

Fig. 4. Digital phase detector timing diagram.

lead of the output amplifier to produce a plus or minus voltage.

Limitations

The upper limit of operation is governed by the stability that can be achieved with a heterodyne principle of operation. Crystal controlled oscillators are available at 600 MHz, and easily can be cut to 0.1 MHz. The exact frequency is not important as long as it is stable. Variations in oscillator frequency will appear as phase shift errors in the system. A standard double balanced mixer is readily available and, being a passive device, does not represent a basic limitation.

Beyond the mixers, the system is the same, regardless of basic operating frequency. The count-frequency used depends on the basic resolution desired; that is, degrees per pulse. The bandwidth is governed by the heterodyne oscillator frequency. Based on the equation previously developed, if the bandwidth can be reduced, the count frequency rate also can be reduced without sacrificing resolution.

Results

Figure 5 shows four typical traces for a 160° phase shift. The top trace is the output of the LSB. The second trace, the second bit, and so on to the bottom trace that is the fourth bit.

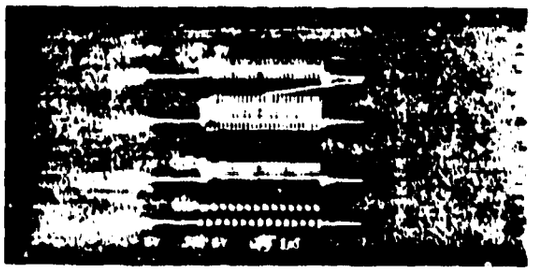

Fig. 5. A 4-bit binary counter output.

Note that there is both a high- and a low-state position on the LSB trace, even though the input phase difference is constant. The simultaneous high- and low-state positions are caused by edge uncertainty, that is, the rise and fall time of the V_Z, on the incoming pulse burst. The end result is that sometimes the LSB will stop high and sometimes low.

Figure 6 is a plot showing the linearity of voltage output vs phase shift. The system was checked against an HP model 840-A vector voltmeter. As can be seen, the present uncertainty in the circuit is ± 3°. This is totally traceable to the edge uncertainty problem.

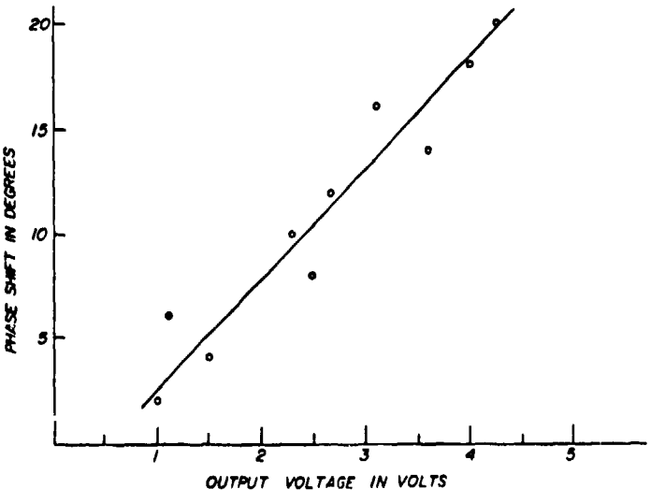

Fig. 6. Phase detector output voltage vs phase shift.

Conclusions

We have shown that it is possible to use digital techniques to measure phase shift with good bandwidth and with good resolution over ± 180°. The system can be used at least up to a basic system frequency of 600 MHz. It may be used at higher frequencies, provided a stable heterodyne frequency source is available. The major limitation of the approach is linearity because of the rise and fall time of the edges of the 100-kHz pulse representing the phase shift.

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